Discrete-time Framework for Digital Control Design in a High-frequency Dual Active Bridge Converter

Avishek Pal, Santanu Kapat, *Senior Member, IEEE*
Embedded Power Management Lab.
Department of Electrical Engineering
Indian Institute of Technology Kharagpur - 721302, India
Email: avishekpal91@gmail.com, skapat@ee.iitkgp.ernet.in

Kapil Jha and Arvind Tiwari
Power Conversion Systems Lab.
GE Global Research
Bengaluru - 560066, India
Email: kapil.jha@ge.com, arvind.tiwari1@ge.com

***Abstract*—Dual active bridge (DAB) converters have been gaining increasing popularity in the context of high-frequency solid state transformers. However, modeling of a DAB converter remains a challenge to retain the ripple information for the design of high performance stable digital control under uniform sampling. This paper proposes a discrete-time framework using approximate discrete-time models considering various practical parasitics. These models are used to derive various discrete-time small-signal transfer functions under phase shift modulation using both voltage mode and current mode control techniques. The accuracy of the proposed models is verified through SIMPLIS simulation as well as experimentation in time-domain and in the frequency domain using SIMPLIS simulation. Finally, a design case-study using digital voltage-mode control is considered for a prototype DAB converter under phase-shift modulation with a power rating of 50 W and switching frequency of 500 kHz. The digital controller is implemented using an FPGA device, and the test results are demonstrated. The proposed framework can be extended to different modulation techniques as well as other isolated DC-DC converter topologies to design high frequency digital control.**

I. Introduction

A bidirectional dual active bridge (DAB) converter emerges as the promising DC transformer as well as the key element in a solid state transformer. A DAB finds widespread applications, such as DC transformer in active cell balancing [1], PV micro inverters [2], medium voltage solid state transformers [3]– [4], smart grids [5], etc. A DAB converter offers various features in terms of low device and component stress, small filter components, low sensitivity to system parasitics and low switching losses by virtue of zero voltage switching. Therefore, a high-frequency DAB converter can achieve high power density with reduced switching losses. It also enables the bidirectional power flow and provides the galvanic isolation with effective transformer core utilization.

The DAB converter was first reported in [6] as a three phase soft switched DC-DC converter topology for a high power application, in which the power flow characterization and the soft switching boundary were discussed. The impacts of snubber capacitance and magnetizing inductance of the transformer on the soft switching operating region along with various control schemes of a DAB converter were reported in [7]. A DAB converter requires closed-loop control to regulate its output voltage and/or current depending on applications; thus various small-signal transfer functions are needed to design the controller. Since the (steady-state) average value of the inductor (or the transformer) current remains zero over the switching time period, a classical state-space averaging technique [8] often fails to accurately capture small-signal dynamics of a DAB converter. A generalized averaging technique [9] was applied for modeling a DAB converter, and the frequency response of the control-to-output transfer function was experimentally verified in [10]. However, this approach yields highly complex expressions which fails to provide any physical insight for the controller design. A small-signal modeling approach was reported in [11] for isolated bidirectional DC-DC converters under different modulation schemes. An alternative full order modeling approach was proposed for a DAB converter under the phase-shift modulation (PSM) in [12], which can predict the frequency response up to one third of the switching frequency. A reduced-order averaging technique was reported in [13]. A bilinear discrete-time modeling approach in [14] uses matrix exponentials which are then approximated up to first order terms. In this approach, it is difficult to accurately capture the fast inductor current dynamics in presence of the parasitic resistance. Another continuous time average modeling technique was discussed in [15] considering a DAB converter as a two time-scale system. However, the inductor current dynamics was neglected in this approach. State space modeling using an improved first harmonic approximation was presented in [16]. However, most of the modeling approaches were limited to continuous-time control. For digitally controlled DAB converters under uniform sampling, a discrete-time modeling approach was reported in [17] to derive various small-signal transfer functions. While this approach uses matrix exponentials, this works on perturbed dynamics rather than the original dynamics; thus, sub-harmonic instability cannot be captured, particularly for current mode control.

Considering the natural current and voltage dynamics, this paper proposes a discrete-time framework. which can predict both large- and small-signal behavior. This proposed approach is useful for direct digital controller design.

978-1-5386-1180-7/18/$31.00 ©2018 IEEE

II. The Proposed Discrete Time Modeling

The schematic of a DAB converter is shown in Fig. 1(a). This can be viewed as an equivalent RLC circuit as shown in Fig. 1(b) under different switch configurations within a complete switching interval using different combinations of input voltage v_{in} and output voltage v_o. For sake of simplicity, the effects due to transformer magnetizing inductance, core-loss resistance, and switching transients as well as dead time are not considered in the modeling.

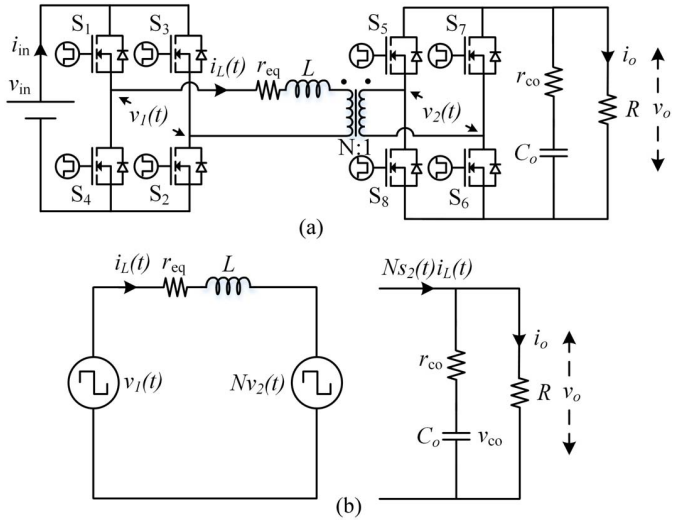

Figure 1. (a) Schematic of a DAB converter with v_{in} and v_{o} as the respective input and output voltages: (b) Equivalent RLC circuit of the DAB converter.

Under phase shift modulation (PSM), the voltages in Fig. 1(b) can be written as $v_1(t) = s_1(t) \times v_{\text{in}}$ and $v_2(t) = s_2(t) \times v_o$, where

$$s_1(t) = \begin{cases} 1 \; for \; 0 \le t \le \dfrac{T_s}{2} \\ -1 \; for \; \dfrac{T_s}{2} \le t \le T_s \end{cases};$$

$$s_2(t) = \begin{cases} 1 \; for \; \dfrac{\varphi T_s}{2} \le t \le \dfrac{(1+\varphi)T_s}{2} \\ -1 \; for \; \dfrac{(1+\varphi)T_s}{2} \le t \le T_s \cup 0 \le t \le \dfrac{\varphi T_s}{2} \end{cases}. \quad (1)$$

Depending on the switch configuration under PSM as shown in Fig. 2(a), there exist four modes which are summarized in Table I. Applying the Kirchhoff's Voltage Law (KVL) to the equivalent RL circuit in Fig. 1(b), it can be written using (1) as

$$\begin{aligned} v_1(t) &= i_L(t)\, r_{\text{eq}} + L\frac{di_L(t)}{dt} + N v_2(t) \\ &\Rightarrow \frac{i_L(t)}{\tau} + \frac{di_L(t)}{dt} = m_k; \\ \tau &= \frac{L}{r_{\text{eq}}}; \;\; m_k = \frac{s_1(t)\, v_{\text{in}} - N s_2(t)\, v_0}{L}, \end{aligned} \quad (2)$$

where m_k indicates the slope of the inductor current related

Table I
States of Switches under Four Different Modes

Modes	ON State	OFF State
Mode-1	S_1, S_2, S_7 and S_8	S_3, S_4, S_5 and S_6
Mode-2	S_1, S_2, S_5 and S_6	S_3, S_4, S_7 and S_8
Mode-3	S_3, S_4, S_5 and S_6	S_1, S_2, S_7 and S_8
Mode-4	S_3, S_4, S_7 and S_8	S_1, S_2, S_5 and S_6

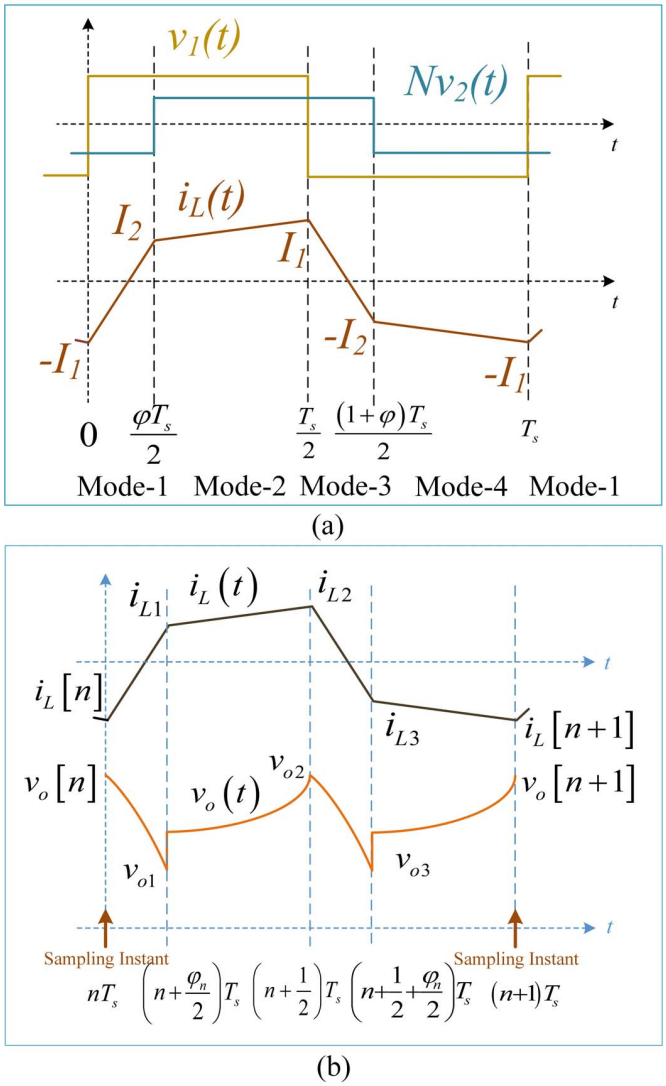

Figure 2. (a) Steady state inductor current under phase shift modulation. (b) Sampling instants for inductor current and output voltage.

to four different modes, r_{eq} is the equivalent resistance which includes the on-time resistance of MOSFET, the DC resistance of the inductor and the winding resistance of the transformer. From (2), the inductor current dynamics with the initial time t_0 and the initial value I_0 can be written as

$$i_L(t) = \tau m_k + (I_0 - \tau m_k)\exp\left(-\frac{t-t_0}{\tau}\right). \quad (3)$$

Similarly, the capacitor voltage dynamics in Fig. 1(b) can be

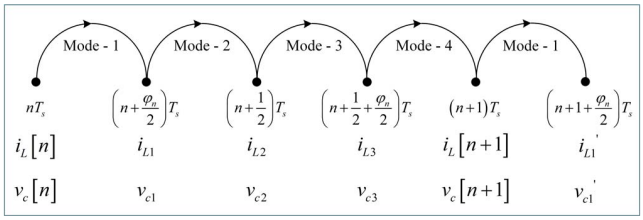

Figure 3. Initial and final values of time and state variables under four respective modes using phase shift modulation.

derived using (2) and (3) with the initial value $v_{\rm co}$ as

$$v_c(t) = \frac{Ns_2(t)\tau}{C_o} m_k (t-t_0) + \frac{Ns_2(t)\tau}{C_o}(I_0 - \tau m_k)\left\{1-\exp\left(-\frac{t-t_0}{\tau}\right)\right\} - \frac{v_o}{RC_o}(t-t_0) + v_{\rm co}. \quad (4)$$

Let $i_L[n]$ and $v_c[n]$ be the inductor current and the capacitor voltage at the beginning of the $n^{\rm th}$ switching interval; and $i_L[n+1]$ and $v_c[n+1]$ be the their respective final values at the end of that switching interval as shown in Fig. 2(b). The periodic switching sequence consisting of different modes is shown in Fig. 3.

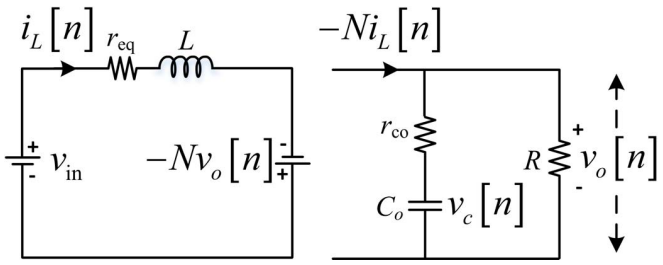

Figure 4. Equivalent RLC circuit of DAB converter at the $n^{\rm th}$ sampling instant.

Under uniform sampling, the output voltage is sampled once in a switching cycle at the instant shown in Fig. 2(b), where $v_o[n]$ is the sampled output voltage at the n^{th} sampling instant. Now, the sampled output voltage $v_o[n]$ at $n^{\rm th}$ sampling instant is considered to compute the different inductor current slopes (m_1 to m_4) under four respective modes throughout the $n^{\rm th}$ switching cycle or until the $(n+1)^{\rm th}$ sample of output voltage being captured. Now, at the n^{th} sampling instant, the equivalent RLC circuit of DAB converter is shown in Fig. 4. From this equivalent circuit, the relation between $v_c[n]$ and $v_o[n]$ can be derived as

$$v_c[n] = Ni_L[n] r_{\rm co} + v_o[n]\left(1+\frac{r_{\rm co}}{R}\right) \quad (5)$$

The initial and final values of time and their corresponding state variables such as inductor current i_L and capacitor voltage v_c are depicted in Fig. 3. Using (2) - (5), the analytical expressions of inductor current i_L and capacitor voltage v_c at the end of each mode are derived as below.

Mode - 1: The slope of inductor current m_1 is

$$m_1 = \frac{v_{\rm in} + Nv_o[n]}{L}. \quad (6)$$

With the initial time nT_s, the inductor current $i_L[n]$, the capacitor voltage $v_c[n]$ and the final time $\left(n+\frac{\varphi_n}{2}\right)T_s$ as shown in Fig. 3, the inductor current $i_{\rm L1}$ and the capacitor voltage $v_{\rm c1}$ at the end of this mode become

$$i_{\rm L1} = \tau m_1 + (i_L[n] - \tau m_1)\exp\left(-\frac{\varphi_n T_s}{2\tau}\right); \quad v_{\rm c1} = -\frac{1}{C_o}\left(N\tau m_1 + \frac{v_o[n]}{R}\right)\left(\frac{\varphi_n T_s}{2}\right) - \frac{N\tau}{C_o}(i_L[n] - \tau m_1)\left\{1-\exp\left(-\frac{\varphi_n T_s}{2\tau}\right)\right\} + v_c[n]. \quad (7)$$

Mode - 2: The slope of inductor current m_2 is

$$m_2 = \frac{v_{\rm in} - Nv_o[n]}{L}. \quad (8)$$

With the initial time $\left(n+\frac{\varphi_n}{2}\right)T_s$, the inductor current $i_{\rm L1}$, the capacitor voltage $v_{\rm c1}$ and the final time $\left(n+\frac{1}{2}\right)T_s$ as shown in Fig. 3, the inductor current $i_{\rm L2}$ and the capacitor voltage $v_{\rm c2}$ at the end of this mode become

$$i_{\rm L2} = \tau m_2 + (i_{\rm L1} - \tau m_2)\exp\left\{-\frac{(1-\varphi_n)T_s}{2\tau}\right\}; \quad v_{\rm c2} = \frac{1}{C_o}\left(N\tau m_2 - \frac{v_o[n]}{R}\right)\left\{\frac{(1-\varphi_n)T_s}{2}\right\} + \frac{N\tau}{C_o}(i_{\rm L1} - \tau m_2)\left[1-\exp\left\{-\frac{(1-\varphi_n)T_s}{2\tau}\right\}\right] + v_{\rm c1}. \quad (9)$$

Mode - 3: The slope of inductor current m_3 is

$$m_3 = -\frac{v_{\rm in} + Nv_o[n]}{L}. \quad (10)$$

With the initial time $\left(n+\frac{1}{2}\right)T_s$, the inductor current $i_{\rm L2}$, the capacitor voltage $v_{\rm c2}$ and the final time $\left(n+\frac{1}{2}+\frac{\varphi_n}{2}\right)T_s$ as shown in Fig. 3, the inductor current $i_{\rm L3}$ and the capacitor voltage $v_{\rm c3}$ at the end of this mode become

$$i_{\rm L3} = \tau m_3 + (i_{\rm L2} - \tau m_3)\exp\left(-\frac{\varphi_n T_s}{2\tau}\right); \quad v_{\rm c3} = \frac{1}{C_o}\left(N\tau m_3 - \frac{v_o[n]}{R}\right)\left(\frac{\varphi_n T_s}{2}\right) + \frac{N\tau}{C_o}(i_{\rm L2} - \tau m_3)\left\{1-\exp\left(-\frac{\varphi_n T_s}{2\tau}\right)\right\} + v_{\rm c2}. \quad (11)$$

Mode - 4: The slope of inductor current m_4 is

$$m_4 = -\frac{v_{\rm in} - Nv_o[n]}{L}. \quad (12)$$

With the initial time $\left(n+\frac{1}{2}+\frac{\varphi_n}{2}\right)T_s$, the inductor current $i_{\rm L3}$, the capacitor voltage $v_{\rm c3}$ and the final time $(n+1)T_s$ as shown in Fig. 3, the inductor current $i_L[n+1]$ and the

capacitor voltage $v_c[n+1]$ at the end of this mode become

$$\begin{aligned} i_L[n+1] &= \tau m_4 + (i_{L3} - \tau m_4)\exp\left\{-\frac{(1-\varphi_n)T_s}{2\tau}\right\}; \\ v_c[n+1] &= -\frac{1}{C_o}\left(N\tau m_4 + \frac{v_o[n]}{R}\right)\left\{\frac{(1-\varphi_n)T_s}{2}\right\} - \\ &\quad \frac{N\tau}{C_o}(i_{L3} - \tau m_4)\left[1 - \exp\left\{-\frac{(1-\varphi_n)T_s}{2\tau}\right\}\right] + v_{c3}. \end{aligned} \tag{13}$$

Considering possible practical parasitics, the solutions of the inductor current and the capacitor voltage dynamics are obtained. A second-order approximation of individual dynamics is found to be sufficient to capture the fast-scale behaviour of the converter. Thus, the complete discrete-time model can be derived, sequentially combining these inductor current and capacitor voltage dynamics under respective four modes, which can be written as

$$\begin{aligned} &i_L[n+1] = k_1 v_{\text{in}} + k_2(1-2\varphi_n)v_c[n] \\ &+ [k_3 - k_4(1-2\varphi_n)]\, i_L[n], \\ &v_c[n+1] = k_5\varphi_n(1-\varphi_n)v_{\text{in}} + k_6 v_c[n] \\ &+ [k_7 + k_8(1-2\varphi_n)]\, i_L[n]. \end{aligned} \tag{14}$$

where $k_1 = -\frac{{T_s}^2}{4\tau L}; k_2 = -\frac{Nk_1}{\alpha}; k_3 = e^{-(T_s/\tau)};$
$k_4 = Nr_{\text{co}}k_2; k_5 = \frac{N{T_s}^2}{2LC_o}; k_6 = \frac{r_{\text{co}}NT_s}{\alpha RC_o}; k_7 = \frac{r_{\text{co}}k_5}{2},$
$k_8 = 1 - \frac{T_s}{\alpha RC_o}$, and $\alpha = 1 + \frac{r_{\text{co}}}{R}$. T_s is the switching period. Now using (14), steady state values of the inductor current I_L and the capacitor voltage V_c can be obtained by solving $i_L[n+1] = i_L[n]$ and $v_c[n+1] = v_c[n]$, which are written as

$$\begin{aligned} I_L &= \frac{V_{\text{in}}[k_2k_5\Phi(1-\Phi)(1-2\Phi) + k_1(1-k_8)]}{(1-k_8)[1-k_3+k_4(1-2\Phi)] - k_2(1-2\Phi)k_c}, \\ V_c &= \frac{V_{\text{in}}[k_5\Phi(1-\Phi)\{1-k_3+k_4(1-2\Phi)\} + k_1k_c]}{(1-k_8)[1-k_3+k_4(1-2\Phi)] - k_2(1-2\Phi)k_c}. \end{aligned} \tag{15}$$

where $k_c = k_6 + k_7(1-2\Phi)$, Φ and V_{in} are the phase shift and input voltage at steady-state. Applying small perturbations around the operating point $\{\Phi, I_L, V_{\text{in}}, V_c\}$, the perturbed discrete-time models become $\hat{x}_{n+1} = A\hat{x}_n + B\hat{\varphi}_n + P\hat{v}_{\text{in}}$; $\hat{v}_o[n] = C\hat{x}_n$, where

$$\begin{aligned} A &= \begin{pmatrix} k_3 - k_4(1-2\Phi) & k_2(1-2\Phi) \\ k_6 + k_7(1-2\Phi) & k_8 \end{pmatrix}; \\ B &= \begin{pmatrix} 2(k_4I_L - k_2V_c) \\ k_5V_{\text{in}}(1-2\Phi) - 2k_7I_L \end{pmatrix}; \\ P &= \begin{pmatrix} k_1 \\ k_5\Phi(1-\Phi) \end{pmatrix}; \\ C &= \begin{pmatrix} -\frac{Nr_{co}}{\alpha} & \frac{1}{\alpha} \end{pmatrix}; x_n = \begin{pmatrix} i_L[n] & v_c[n] \end{pmatrix}^T. \end{aligned} \tag{16}$$

Consider the parameter set: $V_{\text{in}} = 36$ V, $R = 1.2\ \Omega$, $r_{\text{eq}} = 0.26\ \Omega$, $L = 6.6\ \mu$H, $C_o = 185\ \mu$F, $N = 6$, $T_s = 2\ \mu$sec, $r_{\text{co}} = 1\ m\Omega$. From (16), different discrete-time transfer functions under voltage mode control using PSM are derived as follows

$$\begin{aligned} \frac{\hat{v}_o(z)}{\hat{\varphi}(z)} &= \frac{0.06884z - 0.06346}{z^2 - 1.9086z + 0.9095}; \\ \frac{\hat{v}_o(z)}{\hat{v}_{\text{in}}(z)} &= \frac{0.00122z - 0.00112}{z^2 - 1.9086z + 0.9095}; \\ \frac{\hat{i}_L(z)}{\hat{\varphi}(z)} &= \frac{-0.2538z + 0.252}{z^2 - 1.9086z + 0.9095}; \\ \frac{\hat{i}_L(z)}{\hat{v}_{\text{in}}(z)} &= \frac{-0.006826z + 0.006767}{z^2 - 1.9086z + 0.9095}. \end{aligned} \tag{17}$$

Digital current mode control under phase shift modulation: The digital current mode control (DCMC) of DAB converter under PSM [18] is shown in Fig. 5 and the corresponding

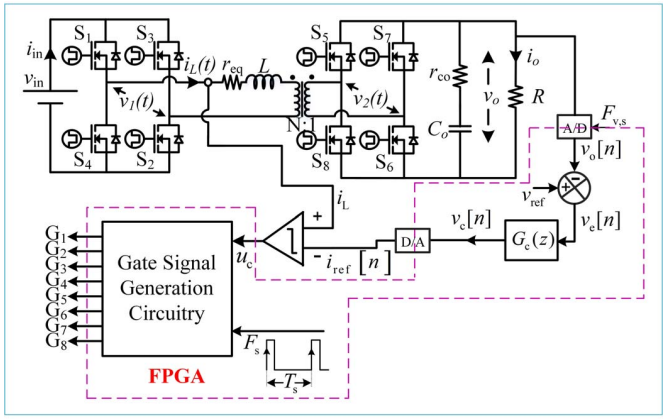

Figure 5. Digital current mode control of DAB converter under phase shift modulation.

inductor current waveform is presented in Fig. 6. Now, $i_{\text{ref}}[n]$

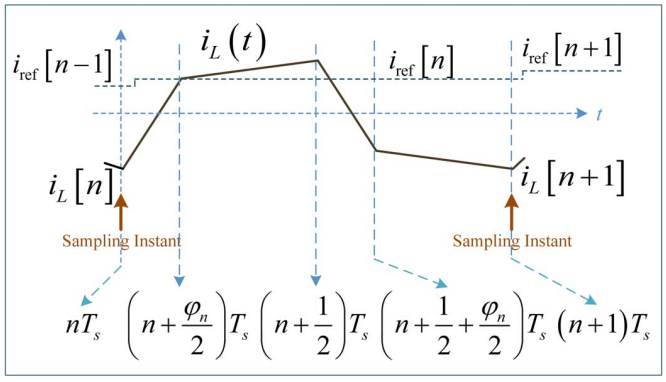

Figure 6. Inductor current using digital current mode control of DAB converter under phase shift modulation.

is generated from outer voltage loop as shown in Fig. 5. Considering second-order approximation of each exponential and using Fig. 6, $i_{\text{ref}}[n]$ can be written in terms of φ_n as

$$\begin{aligned} i_{\text{ref}}[n] &= \frac{\varphi_n T_s}{2\tau\alpha r_{\text{eq}}}\left(1 - \frac{\varphi_n T_s}{4\tau}\right) \\ &(\alpha v_{\text{in}} + Nv_c[n] - i_L[n]\, r_{\text{cons}}) + i_L[n] \end{aligned} \tag{18}$$

where $r_{\text{cons}} = \alpha r_{\text{eq}} + N^2 r_{\text{co}}$. To linearise around the operating

point $\{\Phi,\, I_L,\, V_{\rm in},\, V_c\}$, applying perturbation in (18), the perturbed phase shift $\hat{\varphi}_n$ is expressed as

$$\hat{\varphi}_n = \frac{1}{k_{12}}\hat{i}_{\rm ref}\,[n] - \frac{k_9}{k_{12}}\hat{v}_{\rm in} - \frac{k_{10}}{k_{12}}\hat{v}_c\,[n] - \frac{k_{11}}{k_{12}}\hat{i}_L\,[n] \quad (19)$$

where $k_9 = \dfrac{\Phi T_s}{2\tau r_{\rm eq}}\left(1 - \dfrac{\Phi T_s}{4\tau}\right)$, $k_{10} = \dfrac{Nk_9}{\alpha}$, $k_{11} = 1 - \dfrac{k_9 r_{\rm eq}}{\alpha}$ and $k_{12} = \dfrac{T_s}{2\tau\alpha r_{\rm eq}}\left(1 - \dfrac{\Phi T_s}{2\tau}\right)(\alpha V_{\rm in} + NV_c - I_L r_{\rm cons})$. With the closed inner current-loop, the perturbed model can be derived using (16) by replacing $\hat{\varphi}_n$ in terms of $\hat{i}_{\rm ref}\,[n]\,, \hat{v}_{\rm in}, \hat{v}_c\,[n]$ and $\hat{i}_L\,[n]$ as per (19), which under current mode control becomes $\hat{x}_{n+1} = A_{\rm cl}\hat{x}_n + B_{\rm cl}\hat{i}_{\rm ref}\,[n] + P_{\rm cl}\hat{v}_{\rm in}$; $\hat{v}_o\,[n] = C\hat{x}_n$, where

$$A_{\rm cl} = A - \frac{B}{k_{12}}\begin{bmatrix} k_{11} & k_{10} \end{bmatrix};$$
$$B_{\rm cl} = \frac{B}{k_{12}};\; P_{\rm cl} = P - \frac{k_9}{k_{12}}B. \quad (20)$$

Thus, various discrete-time small-signal transfer functions can be derived under DCMC, which are computed using the parameter set for the nominal switching frequency of 500 kHz and current sense resistance of 10 $m\Omega$, as follows

$$\begin{aligned}
\frac{\hat{v}_o\,(z)}{\hat{i}_{\rm ref}\,(z)} &= \frac{0.866478z - 0.79877}{z^2 - 1.93759z + 0.938478};\\
\frac{\hat{v}_o\,(z)}{\hat{v}_{\rm in}\,(z)} &= \frac{0.000795z - 0.000714}{z^2 - 1.93759z + 0.938478};\\
\frac{\hat{i}_L\,(z)}{\hat{i}_{\rm ref}\,(z)} &= \frac{-0.03194z + 0.03171}{z^2 - 1.93759z + 0.938478};\\
\frac{\hat{i}_L\,(z)}{\hat{v}_{\rm in}\,(z)} &= \frac{-0.005265z + 0.005211}{z^2 - 1.93759z + 0.938478}.
\end{aligned} \quad (21)$$

III. Model Verification and Digital Controller Design

The discrete-time models in (16) and (20) have been verified with SIMPLIS simulation both in time and frequency domain. The time domain verifications are shown in Fig. 7, under step transient in load resistance [in Fig. 7(a)], phase shift [in Fig. 7(b)] and input voltage [in Fig. 7(c)], considering the parameters set in Sec. II. The frequency domain validations under both voltage and current mode control are presented in Fig. 8 up to half of the switching frequency (or the Nyquist frequency) i.e 250 kHz. In Fig. 8, a phase mismatch is found near the Nyquist frequency, which can be compensated by incorporating higher order series expansion of the exponentials in (3) and (4). However, this would increase the model complexity. For target control bandwidths of $1/10^{\rm th}$ under voltage mode control and of $1/5^{\rm th}$ under current mode control with respect to the switching frequency f_s, both the gain and phase plots are accurately matching with the SIMPLIS simulation as shown in Fig. 8. Thus, these reduced-order discrete time models are accurate enough for direct digital control design.

The control-to-output transfer function of the open-loop DAB converter results in 5 kHz bandwidth, i.e., $f_s/100$ and 15 dB DC gain. These would indicate sluggish (over-damped)

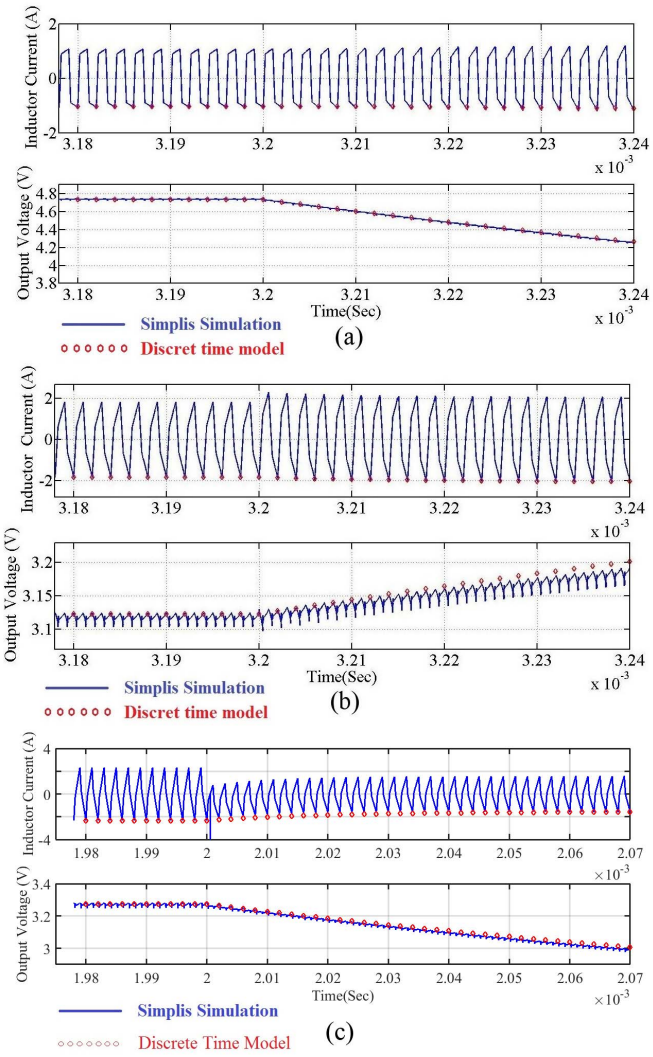

Figure 7. Time domain verification at 36 V input due to step changes in (a) load resistance from 2 Ω to 1.2 Ω (b) phase shift (Φ) from 0.3 to 0.38 (c) input voltage from 40 V to 30 V with load resistance (R) of 2 Ω and phase shift (Φ) of 0.24.

response to reference transient. This observation can also be inferred from the topology itself as there are only capacitors, followed by the load side bridge. For improved performance, a closed-loop discrete-time PI controller $C(z) = k_p + \dfrac{k_i}{1 - z^{-1}}$ is designed using MATLAB SISO toolbox for the desired closed-loop bandwidth of 50 kHz with 60 degree phase margin. The controller gains are found to be $k_p = 13.25$ and $k_i = 0.5$ and the transient response is shown in Figure 11(a).

Under digital current mode control, the control-to-output transfer function yields 70 kHz bandwidth and 63 degree phase margin, which results a fast response to a step load transient. Therefore, a DAB converter is better suited to constant voltage applications which require very fast load transient response. For a target closed-loop bandwidth of $f_s/5$ and 60 degree phase margin, the voltage controller gains are found to be

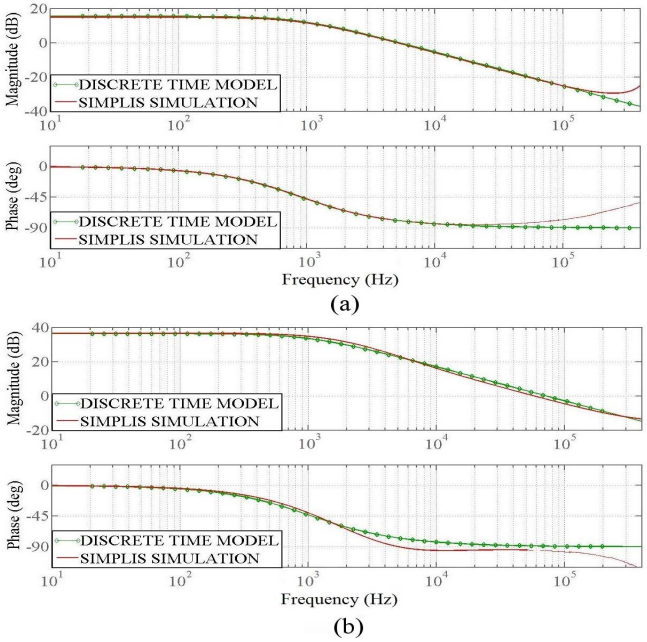

Figure 8. Discrete-time control-to-output transfer function of the DAB converter under phase shift modulation (a) voltage mode control and (b) current mode control.

$k_p = 1.35$ and $k_i = 0.0165$. This indicates that current mode control can achieve faster response compared to voltage mode control even using smaller controller gains, however, at the cost of additional current-loop and the current sensing circuit.

IV. Hardware Implementation

A DAB converter prototype, including signal conditioning circuitry for digital control design has been made as shown in Fig. 10, and the controller is implemented using an FPGA device. The specifications for the hardware prototype are considered as: $v_{\text{in}} \in \{30, 60\}$ V, $v_o \in \{2, 5\}$ V, and nominal $f_s = 500$ kHz using $L = 6.6$ μH, and the transformer

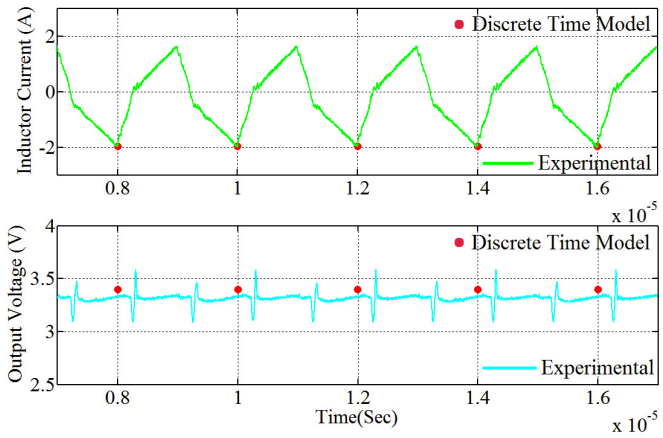

Figure 9. Experimental validation of the model under steady state with V_{in} of 36 V, R of 1.2 Ω and Φ of 0.22. Time scale : 2 μs/div.

turns ratio $N = 6$, and $C_o = 185$ μF. The high frequency

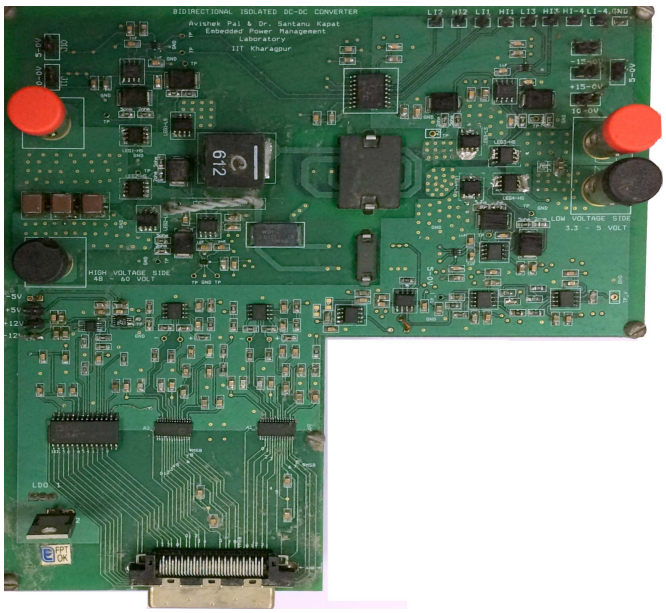

Figure 10. Hardware prototype of Dual Active Bridge converter including the signal conditioning circuitry.

transformer is made of printed circuit board (PCB) traces as transformer winding with planar cores (FERROXCUBE make E22/6/16/R-3F4 and PLT22/16/2.5/S-3F4). A four channel high speed digital isolator (ADUM140D1BRWZ) is used to isolate the gate signals to source and load side bridges. The output voltage is sampled using an ADC (AD9215) once in a switching cycle. The sampled inductor current and output voltage using the proposed models are plotted with the test results, collecting the .CSV files from oscilloscope as shown in Fig. 9 at $v_{\text{in}} = 36$ V, $R = 1.2\,\Omega$, and $\Phi = 0.22$. This figure indicates a close agreement of the derived models with the test results. Figure 11(a) demonstrates the transient performance of the DAB converter using digital voltage mode control using $k_p = 13.25$ and $k_i = 0.5$ for a step change in reference voltage from 1.9 V to 2.7 V, and back at $v_{\text{in}} = 36$ V and $R = 1.2\,\Omega$. Figure 11(b) and (c) show the zoomed version of the step-down and step-up transient respectively. Test results are found to be consistent with the design requirements.

V. Conclusion

A discrete-time framework was proposed in a digitally controlled DAB converter, and the accuracy of the proposed models were verified through experimentation as well as using SIMPLIS simulation. The proposed modeling extends natural responses of the inductor current and the output voltage. These models can be used to derive analytical stability conditions and to obtain various small-signal transfer functions. The proposed approach is simple and useful to other modulation techniques of DAB converter as well as different isolated DC-DC converters.

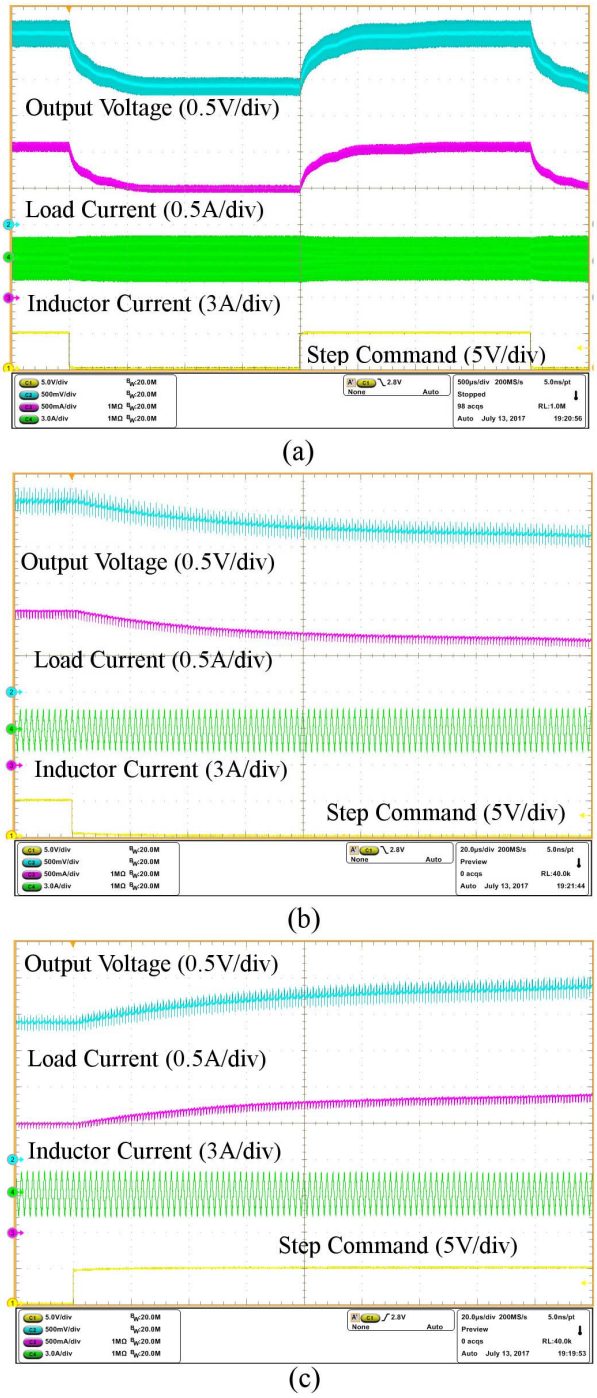

Figure 11. (a) Reference transient from 1.9 V to 2.7 V with v_{in} of 36 V, R of 1.2 Ω, k_p of 13.25 & k_i of 0.5. (b) Zoomed version of (a) under step down and (c) under step up reference transient. Time scale : 500 μs/div in (a) & 20 μs/div in (b) & (c).

ACKNOWLEDGMENT

This work was carried out at the Embedded Power Management Lab., Department of Electrical Engineering, Indian Institute of Technology Kharagpur, with a General Electric funded project.

The leading author would like thank Mr. B G Tilak Vangalapudi for helping in the hardware implementation.

REFERENCES

[1] M. Evzelman, M. M. Ur Rehman, K. Hathaway, R. Zane, D. Costinett and D. Maksimovic, "Active Balancing System for Electric Vehicles With Incorporated Low-Voltage Bus," *IEEE Transactions on Power Electronics,* vol. 31, no. 11, pp. 7887-7895, Nov. 2016.

[2] H. S. Kim, M. H. Ryu, J. W. Baek and J. H. Jung, "High-Efficiency Isolated Bidirectional AC-DC Converter for a DC Distribution System,"*IEEE Transactions on Power Electronics,* vol. 28, no. 4, pp. 1642-1654, April 2013.

[3] S. Bhattacharya, T. Zhao, G.Wang, S. Dutta, S. Baek,Y.Du, B. Parkhideh, X. Zhou, and A. Q. Huang, "Design and development of generation-I silicon based solid state transformer," in Proc. 25th Annu. *IEEE Appl. Power Electron. Conf. Expo.,* Palm Springs, CA, 2010, pp. 1666–1673.

[4] J. Shi, W. Gou, H. Yuan, T. Zhao, and A. Huang, "Research on voltage and power balance control for cascaded modular solid-state transformer," *IEEE Trans. Power Electron.,* vol. 26, no. 4, pp. 1154–1166, Apr. 2011.

[5] S. Inoue and H. Akagi, "A bidirectional isolated dc-dc converter as a core circuit of the next-generation medium-voltage power conversion system," *IEEE Trans Power Electron.,* vol. 22, no. 2, pp. 535–542, 2007.

[6] R. W. A. A. De Doncker, D. M. Divan and M. H. Kheraluwala, "A three-phase soft-switched high-power-density DC/DC converter for high-power applications,"*IEEE Transactions on Industry Applications,* vol. 27, no. 1, pp. 63-73, Jan/Feb 1991.

[7] M. N. Kheraluwala, R. W. Gascoigne, D. M. Divan and E. D. Baumann, "Performance characterization of a high-power dual active bridge DC-to-DC converter,"*IEEE Transactions on Industry Applications,* vol. 28, no. 6, pp. 1294-1301, Nov/Dec 1992.

[8] R. W. Erickson and D. Maksimovic, " Fundamentals of Power Electronics," 2nd ed. New York: Springer-Verlag, 2001.

[9] S. R. Sanders, J. M. Noworolski, X. Z. Liu and G. C. Verghese, "Generalized averaging method for power conversion circuits,"*IEEE Transactions on Power Electronics,* vol. 6, no. 2, pp. 251-259, Apr 1991.

[10] H. Qin and J. W. Kimball, "Generalized Average Modeling of Dual Active Bridge DC–DC Converter,"*IEEE Transactions on Power Electronics,* vol. 27, no. 4, pp. 2078-2084, April 2012.

[11] F. Krismer and J. W. Kolar, "Accurate Small-Signal Model for the Digital Control of an Automotive Bidirectional Dual Active Bridge,"*IEEE Transactions on Power Electronics,* vol. 24, no. 12, pp. 2756-2768, Dec. 2009.

[12] C. Zhao, S. D. Round and J. W. Kolar, "Full-order averaging modelling of zero-voltage-switching phase-shift bidirectional DC-DC converters,"*IET Power Electronics,* vol. 3, no. 3, pp. 400-410, May 2010.

[13] K. Zhang, Z. Shan and J. Jatskevich, "Large and Small-Signal Average-Value Modeling of Dual-Active-Bridge DC–DC Converter Considering Power Losses,"*IEEE Transactions on Power Electronics,* vol. 32, no. 3, pp. 1964-1974, March 2017.

[14] L. Shi; W. Lei; Z. Li; J. Huang; Y. Cui; W. Yue, "Bilinear Discrete-Time Modeling and Stability Analysis of the Digitally Controlled Dual Active Bridge Converter,"*IEEE Transactions on Power Electronics,* vol.PP, no.99, pp.1-1.

[15] Hua Bai, Chunting Mi, Chongwu Wang and S. Gargies, "The dynamic model and hybrid phase-shift control of a dual-active-bridge converter," 2008 34th Annual Conference of *IEEE Industrial Electronics, Orlando, FL,* 2008, pp. 2840-2845.

[16] S. S. Shah and S. Bhattacharya, "Large & small signal modeling of dual active bridge converter using improved first harmonic approximation,"*IEEE Applied Power Electronics Conference and Exposition (APEC),* Tampa, FL, 2017, pp. 1175-1182.

[17] D. Costinett, R. Zane and D. Maksimovic, "Discrete-time small-signal modeling of a 1 MHz efficiency-optimized dual active bridge converter with varying load,"*2012 IEEE 13th Workshop on Control and Modeling for Power Electronics (COMPEL),* Kyoto, 2012, pp. 1-7.

[18] S. Dutta, S. Hazra and S. Bhattacharya, "A Digital Predictive Current-Mode Controller for a Single-Phase High-Frequency Transformer-Isolated Dual-Active Bridge DC-to-DC Converter,"*IEEE Transactions on Industrial Electronics,* vol. 63, no. 9, pp. 5943-5952, Sept. 2016.